REMARKS

Claims 1, 2, and 5-6 and 25 are presently pending in the application. Claims 7-24 have been withdrawn from consideration as being directed to a non-elected invention, Claims 3-4 canceled, and Claim 25 added.

However, the Applicant respectfully points out to the Examiner that Claims 7-24 were canceled in the Preliminary Amendment dated July 25, 2001. Accordingly, Claims 7-24 should be considered canceled by the Examiner.

The Examiner has objected to Claims 2-6 due to informalities. Claims 3-4 have been canceled. Claims 2 and 5-6 have been amended to obviate any informalities noted by the Examiner.

The Examiner has rejected Claims 1-6 under 35 U.S.C. §112, second paragraph, as being indefinite. Claims 3-4 have been canceled, and Claims 1, 2, and 5-6 have been amended to obviate any indefiniteness noted by the Examiner in impreciseness of claim language.

The Examiner has rejected Claims 1-6 under 35 U.S.C. §103 as being unpatentable over Ito et al. in view of Nishikawa et al. Further, the Examiner has rejected Claims 3-6 under 35 U.S.C. §103 as being unpatentable over Ito et al. and Nishikawa et al. and further in view of Acocella et al. Claims 3 and 4 have been canceled, and the limitations of Claim 3 included in Claim 1 to further clarify the invention. For the following reasons, the prior art rejections are respectfully traversed.

The Applicant respectfully submits that neither Ito et al. nor Nishikawa et al. teaches or suggests a semiconductor device wherein said metal bumps are solder bumps and solder layers different in composition from said solder bumps are formed at the surfaces of the solder bumps projecting out from the resin film, as recited in amended Claim 1.

Rather, Ito et al. and Nishikawa et al. are silent with respect to solder layers of different composition from the solder bumps being disposed on the solder bumps. Further, Nishikawa et al. disclose only oxide/contamination layers 6 coating the surface of the solder balls 2, and are silent with respect to solder layers being disposed on the solder bumps.

Accordingly, Claim 1 is not obvious over either the individual or the combination of the Ito et al. and Nishikawa et al. references, and the rejection of Claim 1 under 35 U.S.C. §103 should be withdrawn.

Further, since Claims 2 and 5-6 depend from Claim 1, they are also patentably distinguishable over either the individual or the combination of the Ito et al., Nishikawa et al., and Acocella et al. references for the reasons cited above with respect to Claim 1.

With respect to new Claim 25, the applied prior art does not teach or suggest a semiconductor device including a semiconductor chip wherein upper surfaces of the solder bumps are cleaned of impurities; a eutectic solder layer is disposed on the cleaned upper surfaces of the solder bumps; a precoated solder layer is disposed on the lands; wherein the eutectic solder layer of the solder bumps and the precoated solder layer join the upper surfaces of the solder bumps to the lands of the mounting board such that a stacked structure is obtained.

Accordingly, Claim 25 is patentable.

"No"

If the Examiner believes that there is any issue which could be resolved by a telephone or personal interview, the Examiner is respectfully requested to contact the undersigned attorney at the telephone number listed below.

Applicants hereby petition for any extension of time which may be required to maintain the pendency of this case, and any required fee for such an extension is to be charged to Deposit Account No. 19-3140.

Respectfully submitted,

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14271155/V1

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Page 30, the fourth full paragraph, continuing to page 31, was amended as follows:

In Fig. 6, the plasma treatment device 300 is a so-called triode type RF plasma treatment device comprised of a sealed plasma treatment chamber 301, [a] an anode plate 302 provided at the top inside the plasma treatment chamber 301, a stage 303 serving as a cathode plate provided at the bottom, a lattice electrode 304 provided between the anode plate 302 and the stage 303, a coupling capacitor 305 through which a plasma generation power source 306 is connected to the cathode plate 302, and a coupling capacitor 307 through which a substrate bias power source 308 is connected to the stage 303.

IN THE CLAIMS:

Claims 3-4 were canceled.

The claims were amended as follows:

1. (Amended) A semiconductor apparatus comprising:

metal bumps formed so as to connect to a circuit pattern of a semiconductor device and

a resin film formed on a circuit pattern forming surface of said semiconductor device so as to seal spaces between the metal bumps and [become thinner] be lower in height than [the] a height of the metal bumps, the surfaces of the metal bumps projecting out from the resin film being cleaned;

wherein said metal bumps are solder bumps and solder layers different in composition from said solder bumps are formed at the surfaces of the solder bumps projecting out from the resin film.

2. (Amended) [A] The semiconductor apparatus as set forth in claim 1, wherein the surfaces of the metal bumps projecting out from the resin film are cleaned of components [inviting] causing a rise of a connection resistance and a drop in a joint strength at least at connection interfaces.

5. (Amended) [A] The semiconductor apparatus as set forth in claim [3] 1, wherein said solder bumps are comprised of high melting point solder and said solder layer is comprised of eutectic solder.

6. (Amended) [A] The semiconductor apparatus as set forth in claim [4] 2, wherein said solder bumps are comprised of high metal point solder and said solder layers are comprised of a eutectic solder.

Claim 25 was added.